PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 6,868,013	)	Serial No. 10/622,744
	)	
Inventor(s): Tomoharu TANAKA *et al*	)	Filed: March 15, 2005
	)	
Issue Date: March 15, 2005	)	Attorney Docket No. 001701.00193

For: SEMICONDUCTOR MEMORY DEVICE

REQUEST FOR CERTIFICATE OF CORRECTION

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building, Mail Stop: Certificate of Correction Branch
401 Dulany Street
Alexandria, VA 22314

Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322, this is a request for the issuance of a Certificate of Correction in the above-identified patent. Two (2) copies of PTO Form 1050 are appended. The complete Certificate of Correction involves one page.

The mistake identified in the appended Form occurred through no fault of the Applicants, as clearly disclosed by the records of the application, which matured into this patent. Enclosed for your convenience is the relevant portion of the Preliminary Amendment filed July 21, 2003.

Issuance of the Certificate of Correction containing the correction is respectfully requested. Since this change is necessitated through no fault of the Applicants, no fee is believed to be associated with this request. Nonetheless, should the Patent and Trademark Office determine that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: November 14, 2004

By: _____
Steve S. Chang
Registration No. 42,402

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Washington, D.C. 20001
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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 6,868,013

DATED: March 15, 2005

INVENTOR(S): Tomoharu TANAKA *et al*

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 26, Claim 7, Line 35:
Please replace "arid" with --and--

Mailing Address of Sender:

Banner & Witcoff, Ltd.
11th Floor
1001 G Street, N.W.
Washington, DC 20001-4597

FORM PTO 1050 (Rev.2-93)

U.S. PAT. NO 6,868,013

No. of add'l copies
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☒ PATENT ☐ DESIGN B&W Ref. 001701.00193 Date July 21, 2003

☐ HAND CARRY Group/Section ____ Bldg ____ Rm ____

Serial/Patent No. TBA Atty/Sec SSC/eis

Inventor Tomoharu Tanaka et al. Client Suzuye & Suzuye

Title Semiconductor Memory Device

The following has been received in the U.S. Patent and Trademark Office on the date stamped hereon:

- ☒ 46 total pp Spec. including: # of Claims 15 (# of independent claims 2); ☒ Abstract
- ☒ Drawings: ☒ Formal ☐ Informal # of distinct sheets 14 : Figs. 1-16
- ☒ Declaration/Power of Attorney: ☒ Executed ☐ Unexecuted
- ☐ Assignment w/PTO Cover Sheet
- ☒ IDS w/PTO 1449 ☐ References ☐ w/Fee
- ☒ Preliminary Amendment
- ☒ Priority Claim (Foreign or U.S. Provisional. B&W # ____)
  Country Appl. # Date
  ☐ w/Foreign Priority Document(s)
- ☒ Application: ☐ CIP ☒ Continuation ☐ Divisional
  Parent Ser. No. 10315030 B&W# 1701.00171
- ☐ U.S. Provisional ____ pp Spec/Claims; Cover Sheet
- ☐ Response to Missing Parts/Requirements dtd ____
- ☐ Response to Notice to File Corrected Applin. Papers dtd ____
- ☐ Request for Expedited Foreign Filing License
- ☐ Request for Corrected: ☐ Filing Receipt ☐ Assignment
- ☐ Response to Restriction/Election Requirement
- ☐ Sequence Listing: ☐ Diskette ☐ Paper
- ☐ Amendment ☐ Response: OA dtd ____
- ☐ Petition for Extension of Time until ____
- ☐ CPA ☐ RCE ☐ w/Ext of Time: OA dtd ____
- ☐ Request for Approval of Drawing Changes
- ☐ Notice of Appeal & Fee
- ☐ Brief: ☐ Appeal & Fee ☐ Reply
- ☐ Request for Oral Hearing
- ☐ Issue Fee ☐ Advance Patent Copies (# ordered) ____
  Notice of Allowance dtd ____
- ☐ Amendment under 37 CFR 1.312
- ☐ Request for Certificate of Correction
- ☒ Transmittal ☒ Fee Transmittal w/Auth. to Charge Deposit Acct.
- ☐ Certificate of Mailing
- ☐ Check # ____ for $ ____
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(4)

☒ PATENT ☐ DESIGN B&W Ref. 001701.00193 Date July 21, 2003

☐ HAND CARRY Group/Section ____ Bldg ____ Rm ____

Serial/Patent No. TBA Atty/Sec SSC/eis

☒ PATENT ☐ DESIGN B&W Ref.: 001701.00193

RETURN WHEN SERIAL NUMBER IS ASSIGNED TO APPLICATION

USPTO: Please return this card, indicating receipt date and Application Serial No. of the following patent application:

Applicant(s): Tomoharu Tanaka, Hiroshi Nakamura, Toru Tanzawa

Title: Semiconductor Memory Device

OB306 U.S. PTO 10/622744 07/21/03

Filing Date: July 21, 2003

Client: Suzuye & Suzuye

Attorney/Secretary: SSC/eis Client Ref.: T2SN-97S0742-D2C3

B&W Rev 5/01

NOV 21 2005

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Tomoharu TANAKA et al.	
Serial No.: TBA; (Rule 53(b) Continuation Application of SN 10/315,030)	Group Art Unit: 2824 (parent) Examiner: Son T. Dinh (parent)
Filed: herewith	Atty. Docket No.: 001701.00193
For: SEMICONDUCTOR MEMORY DEVICE	

PRELIMINARY AMENDMENT

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to initial examination, please amend the above-captioned Continuation application as follows:

In The Specification:

Please amend the specification as follows:

On page 1, replace paragraph 1 with the following paragraph:

--This application is a continuation of U.S. application Serial No. 10/315,030, filed December 10, 2002, which is a continuation of U.S. application Serial No. 10/024,189, filed December 21, 2001, now U.S. Patent No. 6,344,996, which is a continuation of U.S. application Serial No. 09/768,588, filed January 25, 2001, which is a divisional of U.S. application Serial No. 09/504,903, filed February 16, 2000, which is now U.S. Pat. No. 6,208,573, and which is a divisional of U.S. application Serial No. 09/055,216, filed April 6, 1998, which is now U.S. Pat. No. 6,064,611.--

voltage as the program inhibition voltage.

15. (New) The device according to claim 12, wherein the memory transistor stores data of more than one bit.

16. (New) The device according to claim 15, wherein the program promotion voltages are dependent on the data to be programmed.

17. (New) The device according to claim 12, further comprising a second select transistor connected to the second terminal of the memory transistor in order to control a current path of the memory transistor, wherein the second select transistor is non-conductive from the first time to the second time.

18. (New) A semiconductor memory device comprising:

a memory unit having a plurality of memory transistors connected in series and having a first end and a second end;

a first select transistor connected to the first end of said memory unit;

a second select transistor connected to the second end of said memory unit;

a bitline connected to the first end of said memory unit through the first select transistor; and

a programming circuit which applies a first voltage to a gate electrode of the first select transistor at a first time of programming, applies a second voltage to a gate electrode of a selected memory transistor in the memory unit at the first time of programming, applies a third voltage to a gate electrode of a memory transistor other than the selected memory transistor in the memory unit at the first time of programming, applies a fourth voltage to the gate electrode of the first select transistor at a second time of programming after the first time, applies a

programming voltage to the gate electrode of the selected memory transistor at the second time of programming, applies a fifth voltage to the gate electrode of the memory transistor other than the selected memory transistor at the second time of programming, applies a program inhibition voltage to the bitline from the first time to the second time when the selected memory transistor is to be prevented from programming, and applies a plurality of program promotion voltages at the second time when the selected memory transistor is to be programmed,

wherein the first voltage is higher than the fourth and program inhibition voltages, the program promotion voltages are lower than the fourth and program inhibition voltages, the second voltage is lower than the programming voltage, and the third voltage is lower than the fifth voltage.

19. (New) The device according to claim 18, wherein the second voltage has a same voltage as the third voltage.

20. (New) The device according to claim 19, wherein the fourth voltage has the same voltage as the second and third voltages.

21. (New) The device according to claim 18, wherein the memory transistor other than the selected memory transistor is positioned between the selected memory transistor and the first select transistor.

22. (New) The device according to claim 21, wherein a memory transistor, which is adjacent to the selected memory transistor and is positioned between the selected memory transistor and the second select transistor, has a gate electrode connected to a ground voltage.

23. (New) The device according to claim 18, wherein the fourth voltage has a same voltage as the program inhibition voltage.